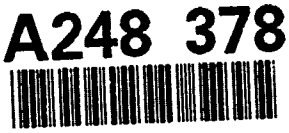

PL-TR-91-2236

PROTOTYPE INSTRUMENTATION AND DESIGN STUDIES

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September 24, 1991

Scientific Report No. 3

PHILLIPS LABORATORY
AIR FORCE SYSTEMS COMMAND
HANSCOM AIR FORCE BASE, MASSACHUSETTS 01731-5000

"This technical report has been reviewed and is approved for publication"

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	24 September 1991	Scientific Report No. 3

4. TITLE AND SUBTITLE
Prototype Instrumentation and Design Studies

5. FUNDING NUMBERS
PE 62101F
PR ILIR TA 7H WU AA

Contract F19628-87-C-0094

6. AUTHOR(S)
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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
AMPTEK, Inc
6 DeAngelo Drive
Bedford, MA 01730

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Phillips Laboratory
Hanscom AFB, MA 01731-5000

Contract Manager: Capt Marilyn Oberhardt/PHP

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
PL-TR-91-2236

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

Flight prototype sensor systems using spherical sections and electrostatic deflection have been developed, fabricated, tested and calibrated. The detectors measure the flux of ions and electrons over a 100° x 10° angular fan and in 32 discrete energy levels from 10 eV to 10 KeV. This report describes the sensor system design for an instrument package for shuttle flight as well as a correlator to look for wave-particle interactions. Operating procedures for a 2.4 Gigabyte Flight Data Recorder are included.

14. SUBJECT TERMS		15. NUMBER OF PAGES
Electrostatic analyzer	Electrons, Particle correlation, Wave-Particle interactions, Plasma analyzer, Flight data recorder	34
Multiangular ESA		16 PRICE CODE
Ions		

17. SECURITY CLASSIFICATION OF REPORT	18 SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	SAR

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Introduction

The third year (September 5, 1989 through September 4, 1990) of the Prototype Instrumentation and Design Studies Contract F19628-87-C-0094 was principally spent in completing and testing the various parts of the Shuttle Potential and Return Electron Experiment (SPREE). Additional efforts were made toward developing a high voltage photodiode and applications of this device in the design of advanced high voltage generation and control circuitry. Much was learned during that period and this report will summarize our results.

High Voltage Supply

Previous years' work has demonstrated the feasibility of using high voltage optocouplers for the control elements in high voltage sweep circuits. The principal concern that remains is the development of packaging and manufacturing techniques to meet spaceflight reliability criteria.

Sources of suitable high voltage diodes and reliable light emitting diodes have been identified. The physical packaging of the high voltage diode is crucial to the overall efficiency of the assembled optocoupler. Proper lead attachment, diode passivation, and glass encapsulation are all vital to the overall efficiency and reliability. Amptek has developed screening and test criteria that can rapidly grade candidate diodes.

The light emitting diodes (LEDs) desired for the control element should have stable and efficient infrared output and predictable directionality to allow optimizing the coupling of the LEDs to the high voltage diode. The LED should be capable of sustained operation over time without severe output degradation or thermal drift.

The mounting materials used for these devices should avoid chemical contamination of the active elements. The LED/high voltage diode interface must be kept optically clear and not be degraded due to color center development or aging. The mount should maintain the relative alignment of the components, mechanically protect the assembly and provide sufficient electrical isolation to accommodate the maximum high voltage rating. Thermal expansion coefficients need to be matched or accommodated. The finished assembly should be simple to handle and mount for the end users.

These problems were thought to be resolved and the SPREE high voltage supply and control circuit was designed and built. Bench testing verified proper operations and the boards were integrated into the electrostatic analyzers. After several days of operation during particle calibration the swept deflection power supply began to lose control of the low voltage portion of the deflection sweep. Table 1 shows the various deflection voltages and their corresponding energy passband. Steps below a few hundred eV were no longer accessible. After cooling overnight the low voltage range was partially recovered but began to fade as the instrument warmed up.

Table 1 headings are N (step number), Energy (center energy of SPREE ESA at this step), E_O (electron outer deflection voltage), E_I (electron inner deflection voltage), I_O (ion outer deflection voltage), I_I (ion inner deflection voltage), and DefMon (Deflection monitor housekeeping output).

N	Energy	Eo	Ei	Io	Ii	DeflMon
31	10000.0	-1971.000	2464.000	2519.000	-3400.000	8.000
30	8002.5	-1577.293	1971.816	2015.830	-2720.851	6.402
29	6404.0	-1262.229	1577.947	1613.169	-2177.361	5.123
28	5124.8	-1010.099	1262.752	1290.938	-1742.434	4.100
27	4101.1	-808.332	1010.518	1033.074	-1394.383	3.281
26	3281.9	-646.868	808.667	826.717	-1115.855	2.626
25	2626.4	-517.656	647.136	661.581	-892.963	2.101
24	2101.7	-414.254	517.871	529.430	-714.594	1.681
23	1681.9	-331.507	414.426	423.677	-571.854	1.346
22	1346.0	-265.289	331.645	339.047	-457.626	1.077
21	1077.1	-212.297	265.399	271.323	-366.216	0.862
20	862.0	-169.891	212.385	217.126	-293.064	0.690
19	689.8	-135.955	169.961	173.755	-234.525	0.552
18	552.0	-108.798	136.012	139.048	-187.678	0.442
17	441.7	-87.066	108.843	111.273	-150.190	0.353
16	353.5	-69.674	87.102	89.046	-120.189	0.283
15	282.9	-55.757	69.703	71.259	-96.182	0.226
14	226.4	-44.620	55.780	57.025	-76.969	0.181
13	181.2	-35.707	44.638	45.634	-61.595	0.145
12	145.0	-28.574	35.722	36.519	-49.291	0.116
11	116.0	-22.867	28.586	29.224	-39.445	0.093
10	92.8	-18.299	22.876	23.387	-31.566	0.074
9	74.3	-14.644	18.307	18.715	-25.261	0.059
8	59.5	-11.719	14.650	14.977	-20.215	0.048
7	47.6	-9.378	11.724	11.985	-16.177	0.038
6	38.1	-7.505	9.382	9.591	-12.946	0.030
5	30.5	-6.006	7.508	7.675	-10.360	0.024
4	24.4	-4.806	6.008	6.142	-8.290	0.020
3	19.5	-3.846	4.808	4.915	-6.634	0.016
2	15.6	-3.078	3.848	3.933	-5.309	0.012
1	12.5	-2.463	3.079	3.148	-4.249	0.010
0	10.0	-1.971	2.464	2.519	-3.400	0.008

TABLE 1 Deflection Voltage for SPREE ESAs

The loss of low voltage control was found to result from thermally induced leakage of the high voltage diode, preventing the HV602 from being entirely turned off. The I-R drop across the diode would elevate the temperature during operation and the leakage would increase. Removing power and allowing the optocoupler to cool recovered most of the dynamic range. Additional sustained operation in a vacuum heated the diode junction once again to an unacceptable leakage level. New models of the high voltage optocouplers that did not have the thermal drift were installed on the board and testing was resumed. This time the leakage problem did not occur; however after several days of continuous operation it was observed that the sweep voltages were no longer able to reach the maximum voltages required for step 31. Troubleshooting

revealed that the LEDs' outputs were degraded to the point that the HV602 could not source enough current to reach maximum output voltage across the load. See Figure 1 for the circuit schematic for this portion of the high voltage supply.

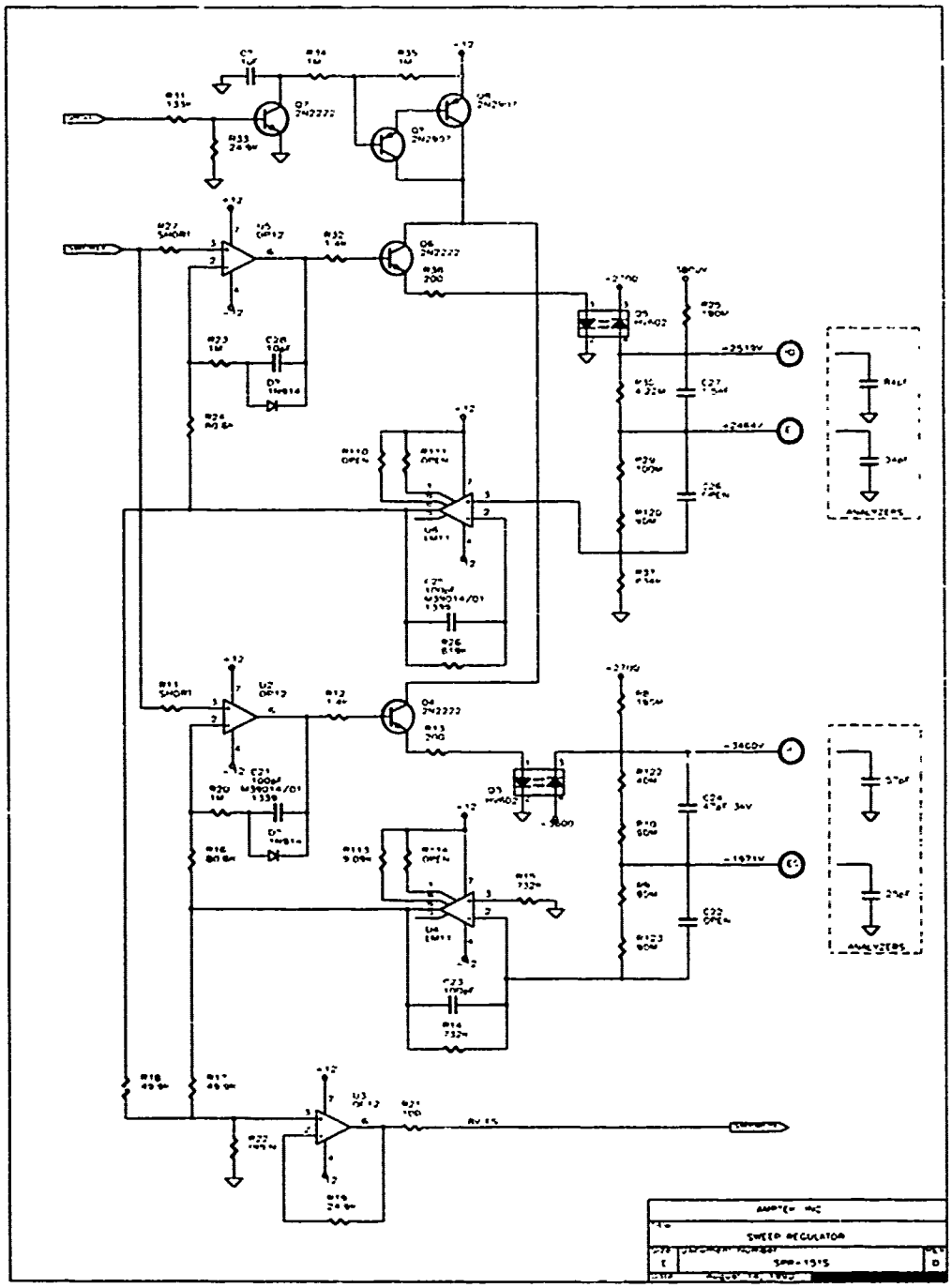


Figure 1 Sweep regulator portion of the SPREE ESA High Voltage Circuit

A review of the SPREE delivery schedule indicated that any further high voltage supply problems would jeopardize the on-time completion of the instrument. In order to maintain the schedule Amptek decided to revert to the type of high voltage optocoupler that we developed and was flown on the CRRES Low Energy Plasma Analyzer (LEPA). This device was similar to the newer HV optocouplers, but consisted of individually screened and tested components that were carefully hand assembled, optimized, and tested. The hand crafted HV optocouplers were installed into the high voltage supply. As of the time of this report, the units have been operated hundreds of hours without any sign of degradation.

A final word about the HV optocouplers. Analysis of the failed units indicated some LEDs' efficiency decline as a result of electrical discharges occurring during the ESA deflection sweep. Tests with other units seem to confirm this analysis and the packaging was changed to separate the LEDs further from the HV diode using light pipes. This remedy appears to prevent this sort of damage. High voltage arcing must be avoided in order to prolong the life of the HV optocouplers and to increase the long term reliability of the high voltage supply. Amptek has continued to develop the HV optocoupler technology using its own resources.

SPREE Log DAC

Another essential component for the high voltage supply was a custom logarithmic digital-to-analog converter (Log DAC). This assembly produces the appropriately scaled voltage steps to control the deflection supply using a clock and reset pulse from the data processor unit for timing. The circuit was designed and packaged in a dual-inline-package (DIP) hybrid for the SPREE experiment. Figure 2 is a schematic of that circuit.

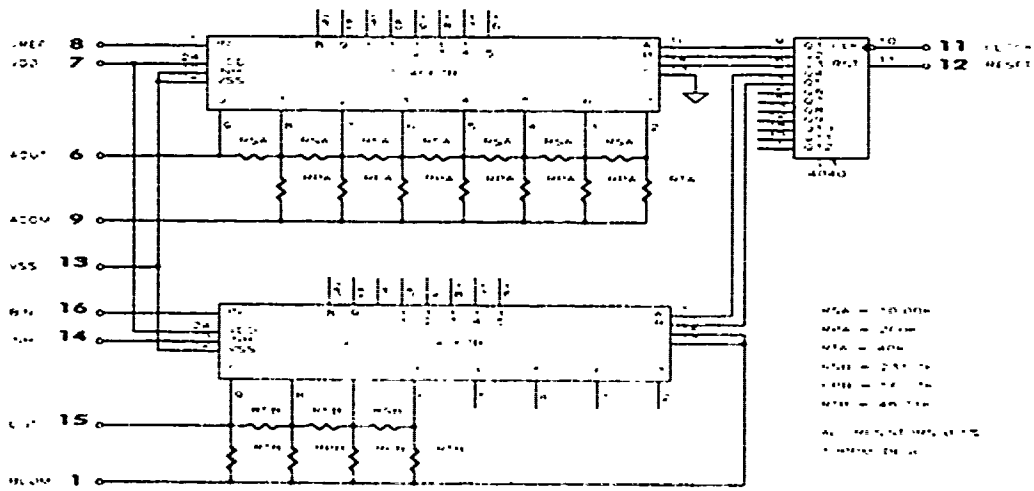


Figure 2 SPREE Log DAC for Sweep Control

Electrostatic Analyzers

Early in this third contract year vibration tests were run on the engineering model of the electrostatic analyzer (ESA). This was a crucial test since it verified whether the microchannel plate (MCP) mounting scheme would survive flight conditions. Each MCP consists of a 0.040 inch thick piece of very brittle and delicate glass. Each sensor has three pairs of these mounted, holding them only at the outer periphery of the MCP. They are expensive long lead-time items that are essential to the ESA design. The engineering ESA passed the vibration tests without harm. Additional testing was then conducted to the limits of the vibration facility (26.3 grms in two axes for one minute each). No damage was sustained; the mounting scheme has been demonstrated mechanically sound.

A series of ion and electron calibrations were conducted on the engineering model. These calibrations verified the energy and angle passbands, gave some preliminary spurious particle rejection data, and generally confirmed the ESA characteristics. The flight models were assembled including the high voltage supply (the engineering model had used external laboratory supplies). Initial tests of the first flight unit revealed an unacceptable noise level. The problem was traced to some low current zener diodes that were used to develop the 200 volts potential difference between the MCP and anode structure. These diodes worked very well but had a high frequency instability just on the knee of their zener curve. Operating these units on a curve tracer revealed a very sharp and noisy knee on all units tested. The zeners were removed and replaced with pairs of 1N4148 signal diodes operating in reverse bias. This arrangement operates in the microampere region and provides a stable bias voltage for the anodes. The noise was reduced to acceptable limits.

After many hours of testing and calibration of the two flight units, some of the angular zones began to show limited response to the calibration source. Troubleshooting revealed that some plated-through vias of the anode structure were poorly manufactured. The vias consist of small (0.020") holes that are coated to electrically interconnect the anode surface to the printed circuit trace on the opposite side of the board. The plating was very thin and non-uniform. The failed anode sectors had apparently lost continuity after repeated thermal cycles induced by the power dissipation of the MCPs. The failure of other sectors seemed probable. The vias were filled with conductive epoxy to reconnect the lost anodes and prevent further loss. The ESAs were reassembled and testing resumed.

Thermal modeling of the ESAs was completed during the period of this report. The original thermal control plan had to be modified to accommodate the screens and screen holder that had been added to the SPREE ESAs. Figure 3 shows a sketch of the resulting thermal control surfaces necessary to stabilize the ESA temperatures while on orbit. The black paint is Chemglaze H322 electrically conductive paint with an emissivity >0.9. The MLI is Indium Tin Oxide Multi-layer Insulation with the electrically conductive side outside. The unpainted surfaces of the housing have been plated with electrodless nickel. Table 2 tabulates some of the predicted extremes of flight temperatures expected under various orbital conditions.

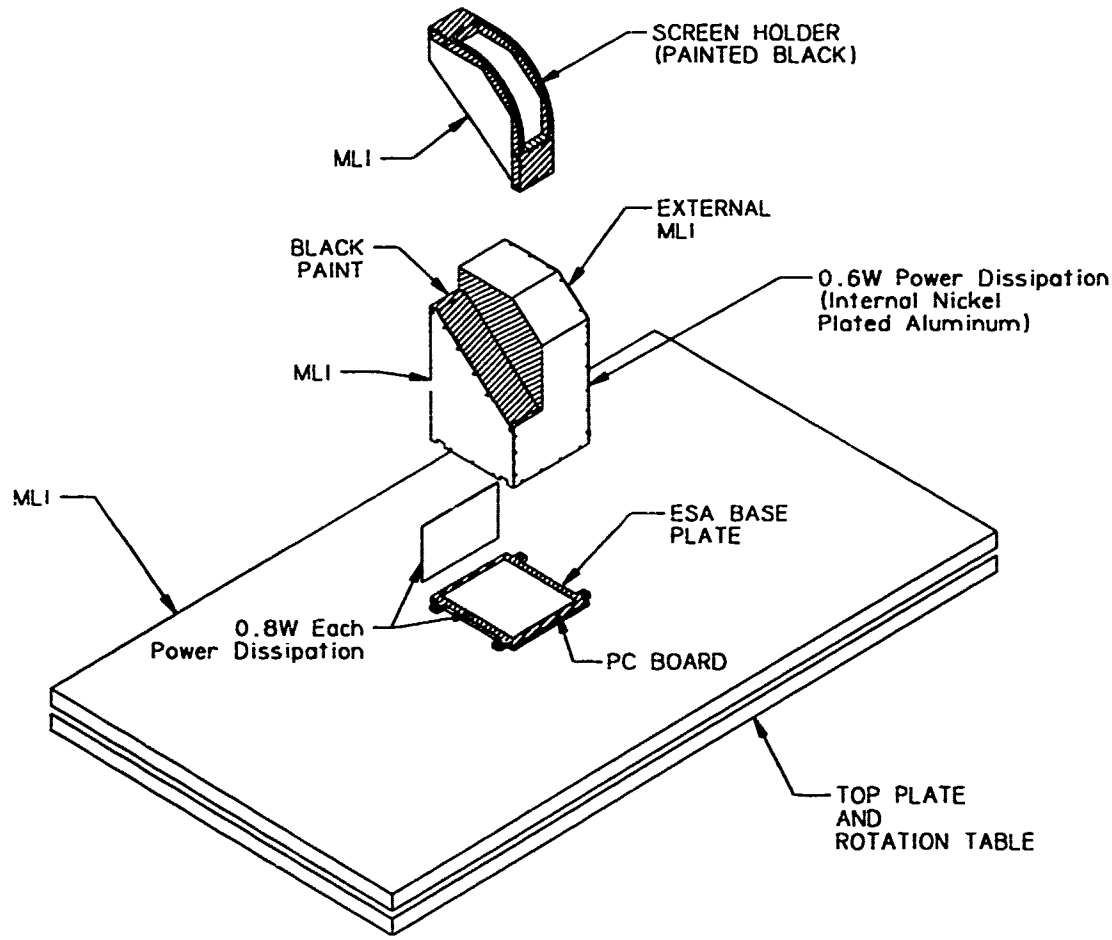


Figure 3 SPREE Electrostatic Analyzer Thermal Control Surfaces

ASSEMBLY	QUALIFICATION LIMITS (OPERATING)	MODEL PREDICTIONS
Flight Data Recorders	-6°C/+50°C	+2°C/+12°C
Data Processing Unit	-20°C/+50°C	+1°C/+19°C
Rotary Table Motor Drive Case	N/A	-3°C/+16°C
Rotary Table Motor	-30°C/+50°C	-3°C/+12°C
ESA Baseplate	-30°C/+50°C	-31°C/+37°C
ESA Aperture/Anode Cover	N/A	-50°C/+37°C
Cold Plate Adapter	N/A	+3°C/+9°C
Top Plate	N/A	+3°C/+17°C

Table 2 SPREE Assemblies Test and Predicted Thermal Extremes

An ESA control box/computer interface unit was designed, built and tested. The box generates and controls the various supply voltages and control signals necessary for the ESAs to operate. It displays instrument currents and has housekeeping monitors. This allows the independent operation of the ESAs without the DPU. It supports testing and calibration. It also included a computer interface to monitor and display all twenty channels of data simultaneously.

A set of dummy loads was built and tested to install inside the ESAs when testing in air so that the high voltage cannot be applied to the microchannel plates. The dummy loads impedances were modeled after the actual MCPs, allowing room pressure testing of the high voltage supply. These units were used during EMI/EMC testing as well as other occasions.

Data Processing Unit

The Data Processing Unit (DPU) was completed during the report period. The DPU consists of several sub-assemblies performing the tasks necessary to control the SPREE hardware and process the data from its sensors. The major sub-assemblies of the DPU are tabulated below with a brief explanation of their principle functions.

Motor Control Board	The motor control board accepts digital stepping pulses and direction (Forward/Reverse) signals from the SPREE primary CPU (via a circuit on the Recorder Interface Board). Each motor is controlled separately and has independent phase quadratured output drivers to power the stepping motor windings. Each circuit (RTMD-A and RTMD-B) can be independently powered through DOH controlled circuitry. The motor output circuit will idle to a low power state if a stepping pulse is not received within 30 milliseconds.
Low Voltage Power Supply	The low voltage power supply consists of three EMI/EMC filters which filter the raw 28 volt primary power. The filter outputs are applied to eight DC/DC inverters which in turn provide the SPREE low voltage power it needs. The inverters are mounted to a specially designed heat sync frame which conducts surplus heat to the DPU base plate and ultimately to the cold plate.
DOH Power Control	The DOH power control board accepts seven DOH bi-levels (28 volts @ 10 milliamps) to switch on and off the SPREE low voltages. Three circuits (DPU, FDR1, and FDR2) directly enable/disable the DC/DC converters. The two motor control DOH signals are optically coupled to transistor switches that control the 15 volt motor drive power. Two circuits switch 28 volt primary power to the HV converter located inside the ESAs.

A/D, HV Control Board	This board provides the analog to digital conversion necessary for encoding housekeeping and the input multiplexer for the converter. It also contains the HV control logic which generates HV step and reset pulses for the two HV circuits housed inside the ESAs.
Recorder Interface Board	This board controls the recorder interfaces for FDR1 and FDR2. It transfers processed data from the experiment to the recorders and monitors the recorders' status signals. It provides an asynchronous interface to the recorders. It also contains the digital logic for generating the motor control step pulses and a PAL that handles the 16 bit to 8 bit log conversion of count rate data.
Telemetry Board	The telemetry board handles the hand shaking protocol with the SFMDM interface. It contains the Digital Input Low (DIL) interface that communicates SPREE status to the SFMDM and a GMT time interface which decodes incoming time code to provide time tagging of the SDIO and Recorder data streams.
Primary CPU Board	The primary CPU supervises the SFMDM SDIO telemetry, DILs, FDR interfaces, and acquires data from the SPACE CPU and auxiliary CPU. It also detects and executes commands and performs error handling chores.
Auxiliary CPU Board	The auxiliary CPU performs the charging algorithm and acquires the count rate data from the accumulator board.
Accumulator Board	The accumulator contains forty 16 bit accumulators that accept the ion and electron zones count data.
SPACE CPU Board	The SPACE CPU over sees the particle correlator functions and SPACE modes. It communicates with the primary CPU to output processed SPACE data. It controls the MCU operations.
SPACE MCU1 Board	This board performs the low frequency autocorrelations on the raw electron counts that are multiplexed from the zone select function.
SPACE MCU2 Board	This board performs the low frequency autocorrelations on the raw ion counts that are multiplexed from the zone select function.
SPACE High Frequency Buncher Board	The high frequency buncher board performs time of arrival correlation analysis on raw electron count rate data looking for high frequency electron bunching. It contains a high frequency crystal clock to time the interval between pulse occurrences.

SPACE Beam Count/ Zone Select Board	This board accepts duty cycle information from SETS and DCORE electron beam operation. It performs correlations of count rate date using these cycles to look for return beam signatures. The zone selector multiplexes the 40 raw count lines to the two MCU boards.
Sensor Interface Board	The sensor interface board provides the interface to the two ESAs. It also contains a high voltage enable circuit that allows the DPU to enable/disable the ESA high voltage in series with the DOH lines. This is a safety protection to avoid inadvertent high voltage turn-on of the MCPs, which would be damaged if operated in air.

The DPU with its three 80C86 CPUs and twelve 80C31 MCUs required a substantial amount of programming and testing to develop code that would perform the necessary tasks and coordinate among themselves. Paul Gough at Sussex University generated most of the MCU code and instructions for the 80C86 SPACE microprocessor. Amptek developed the master control code that directed the two other 80C86 microprocessors. Tests were run between SPACE and the primary experiment. The DPU was transported several times to Huntsville Alabama to test the SFMDM interface. Testing and verification continue as this report period ends.

One problem that was corrected during this period was an under voltage condition that could occur with the FDRs. The FDR recorders require a five volt source with only a 4% tolerance. That means that the --5 volt supply can only vary $\pm$200 millivolts. A special low voltage drop solid state switch was used inside the recorders to minimize line loss. Testing revealed that the printed circuit traces on the recorder interface board, mother board, and power control board could amount to as much as 100 milliohms of resistance. The recorder draws more than 2 amperes of five volt power and the PC trace resistance were dropping too much voltage. The traces were more than adequate to handle the current, but the tight tolerance of the tape recorder made the operation marginal. New circuit layouts were made which used 16 gauge stranded wire busses to carry the five volts. This approach allows enough engineering margin. It should be noted that the most serious voltage drops were occurring on the printed circuit cards, not the several connector pins that the power passed through. The connectors were rated at < 10 milliohms per contact. In all cases two or more contacts had been used to pass the power through a connector. This experience demonstrates that one must be cautious of tight voltage requirements combined with high current loads. A remote voltage sense circuit would have been the ideal solution to this problem. A locally mounted supply would have also worked well.

The SPACE portion of the DPU was a cooperative effort between Amptek and Dr. Paul Gough of Sussex University, United Kingdom. Dr Gough developed the software to be executed in the SPACE portion of the SPREE experiment. A listing of the current correlator algorithms follows:

```
;SPREE-SPACE CPU FOR SHUTTLE TETHER FLIGHT 1991
;        M.P.GOUGH  1 sept 1989
;
;       LAST MODIFIED 19 JUNE 1990
;
;SOURCE= SPACE.ASM
;
;SPREE INSTRUMENT-
; TWO 120 DEGREE ELECTRON SPECTROMETERS A,B
; TWO 120 DEGREE ION SPECTROMETERS A,B
; MOUNTED IN SHUTTLE BAY FOR PLASMA DIAGNOSTICS
; DURING TETHERED SATELLITE & GUN OPERATIONS
; TWO PAIRS ROTATED 180DEGREES/30SEC
; ENERGY STEPPING RATES:
; SLOW- 1 SWEEP/S, FAST- 8 SWEEP/S
;
;SPACE INSTRUMENT-
; SELECTS 3 OFF 10 DEGREE SECTORS FROM EACH
; SPECTROMETER FOR PARTICLE CORRELATION:
; A)HIGH FREQUENCY 0-.625,2.5,10MHz ANALYSIS
;   OF THE SIX ELECTRON PULSE STREAMS,
;   RESOLUTIONS 10,40,160KHz RESPECTIVELY.
; B)LOW FREQUENCY 0-1.25,5.0,10.0KHz ANALYSIS
;   OF ALL TWELVE E+I PULSE STREAMS
;   RESOLUTIONS 38,150,300Hz RESPECTIVELY.
; C)CROSS CORRELATION OF ALL 12 STREAMS AGAINST
;   THE DCOR & FPEG BEAM MODULATION PATTERNS
;
; LOW FREQUENCY-  Fci,Flhr,MIRROR POINT RADAR
; HIGH FREQUENCY- LARMOR PERIOD,Fpe,Fce,
;   SHUTTLE SHEATH/WAKE RADAR
; BEAM CORRELATION-FAST IDENTIFY SOURCES/SINKS
;
;SPACE INSTRUMENT=80C86 CPU AS CONTROLLER,
; 12 X 80C31 MCU AS LOW FREQUENCY ACF,
; 6 X H/W PROCESSORS AS HIGH FREQUENCY ACF,
; 12(+1) PAIRS OF GATED 16BIT COUNTERS FOR BEAM
;
;SPACE CPU CONTROLS LF,HF,&BEAM:
;
;TABLE DRIVEN MODES-
;
;       TIME   ROTATION     ZONES LF          HF
;-----------------------------------------
;       0          1          1,4,7          10KHz          10MHz
        30s        2          2,5,8          10KHz          10MHz
;       60s        3          3,6,9          10KHz          10MHz
;-----------------------------------------
;       90s        4          2,5,8          5KHz           2.5MHz
;       120s       5          3,6,9          5KHz           2.5MHz
;       150s       6          4,7,10         5KHz           2.5MHz
;-----------------------------------------
```

```
;       180s        7          1,4,7          1.25KHz        .625MHz
;       210s        8          2,5,8          1.25KHz        .625MHz
;       240s        9          3,6,9          1.25KHz        .625MHz
;-----------------------------------------
; repeat-
;       270s       10          2,5,8          10KHz          10MHz
; etc..
;
;SPACE CPU OUTPUTS DATA FRAMES TO SPREE
; VIA DUAL PORT RAM:
; LF DATA=12 FRAMES(1096 BYTES EACH)=13152BYTES
; HF DATA=24 FRAMES(1032 BYTES EACH)=24768BYTES
; BEAM DATA=1 FRAME(1672)          = 1672BYTES
; STATISTICAL DATA=1 FRAME (408)   =  408BYTES
;
; FRAME=8BYTES LABEL + DATA
; COMMON LABEL-
; FRAME COUNT(1,2),ROTATION(3),SWEEP(4),ZONE/
; GUN STATUS(5),SLOW-FAST/FREQUENCY RANGE(6),
; NO OF BYTES DATA(7),DATA OFFSET(8)
;
;SLOW STEPPING 1s=8HF+4LF+1BEAM+1STAT=14720BYTE/s
;FAST STEPPING 2s=4HF+4LF+1BEAM+1STAT= 5504BYTE/s
;
;TIME RESOLUTIONS: SLOW          FAST
;-----------------------------------
;   LOW FREQUENCY    3s             6s
;  HIGH FREQUENCY    3s            12s
;    BEAM            1s             2s
;   STATISTICS       1s      2s
;-----------------------------------
;
;CPU INTERRUPT DRIVEN PROGRAM
;1)ENERGY STEP INCREMENT INTERRUPT
;2)DUAL PORT RAM SPREE-> SPACE DATA INTERRUPT
;3)SERIAL DATA READY
;4)WATCH DOG TIMER -> RESET IF HUNG UP [T=1s]
;  RESET BY DATA O/P TO DPR.
;
; BACKGROUND PROGRAM GENERATES STATISTICAL DATA
; WHICH IS ONLY REAL TIME DATA, REST RECORDED.
;
;SPREE-SPACE HANDSHAKE VIA DPR MAIL BOX
;
; SPREE--> SPACE (1BFFCH)
; MS BYTE=
;  FEh-SIGNIFIES SPREE HAS READ DATA IN DPR
;  CXh-NEW ENERGY SWEEP E STEP=0
;
; SPACE--> SPREE (1BFFEH)
; MS BYTE=
;  00h-ACKNOWLEDGES MAIL BOX READ BY SPACE
;
; DPR PARAMETER TABLE:
```

```
; 1BFE0 BX                    SPREE-->SPACE
; 1BFE2 BY                          "
; 1EFE4 BZ                          "
; 1BFE6 A ROTATION            "
; 1BFE8 B ROTATION            "
; 1BFEA        ACKNOWLEDGE        SPACE <--> SPREE
; 1BFEC        CONTROL WORD       SPREE -->SPACE
; 1BFEE        STATUS             SPACE-->SPREE
;
; USE OF DPR PARAMETER TABLE:
;1) AFTER SPACE WRITES 8*N BYTES DATA TO DPR
; SPACE WRITES N TO 1BFEA
; AFTER SPREE READS DATA SPREE WRITES
; 00 TO 1BFEA
; WHEN SPREE WANTS DATA WRITES FE TO MAILBOX
;
;2)CONTROL WORD BITS:
; 0-SENSOR A    MOVING-0 / PARKED-1
; 1-SENSOR B      "      "
; 2-SLOW STEPPING-0 / FAST STEPPING-1
;
;3)STATUS WORD BITS SPACE SELF CHECK RESULT:
; 0     -CPU                GOOD-0 / BAD-1
; 1      -DPR                     "
; 2     -MMU 1                   "
;             :              "
; 13    -MMU 12                  "
;
;CPU-->LF MMU:
; 00XXXXXX ENERGY LEVEL 00-20H 20H=FLYBACK
; 01000YXX XX=FREQUENCY RANGE Y=SLOW/FAST
; 11111111 ALL CLEAR, DATA ALL READOUT
;
;MEMORY MAP
;00000-0FFFFH RAM 32K*16
;10000-107FFH 82C59 INTERRUPT CONTROLLER EVEN
;11000-117FFH 82C54 TIMER 1 UNUSED ODD
;11800-11FFFH 82C54 TIMER 2 ONLY NON FLIGHT ODD
;12000-127FFH LF MCU BOARD 1. MCU1-6
;12800-12FFFH LF MCU BOARD 2. MCU7-12
;13000-137FFH BEAM CROSS CORRELATION
;14000-15FFFH HF BUNCHER
;1B000-1B7FFH WATCH DOG TIMER
;1B800-1BFFFH DUAL PORT RAM 1K*16
;1C000-1FFFFH EPROM 8K*8
;
;RAM USE
;0000-00FF RESET INTERRUPT VECTORS
;0100-01FF PARAMETERS
;0200-08FF BEAM SUMMATION
;0900-0F80 BEAM COPY FOR STATS
;1000-2FFF 4-8 HF FRAME O/P COPY FOR STATS
;3000-3440 LF1 COPY FOR STATS
;3800-3C40 LF2 COPY FOR STATS
```

```
;4000-4440 LF3 COPY FOR STATS
;4800-4C40 LF4 COPY FOR STATS
;5000-5198 STATS O/P FRAME
;6000-7000 STATS SCRATCHPAD
;F000-FFFF STACK
;
;EPROM USE (RELATIVE TO 1C000)
;0000-INT VECTOR TABLE FOR COPYING
;   -OTHER DATA(ZONE SETUPS)
;0100-PROGRAM START
;3FF0-RESET VECTOR (1FFF0)
;
;ES=1000h CS=1C00h DS=0000h
;
;TESTING LEVEL SWITCHES
;======================
NOTFLIGHT           EQU         01H
TIMERS              EQU         00H          ;timers off
WATCHING            EQU         00H          ;watchdog timer off
HFPROTOTYPE         EQU         01H
NOSTATISTICS EQU        01H
;
;EQUATES:
STACKBASE           EQU         0FF00H
MAILRX              EQU         0BFFCH
MAILTX              EQU         0BFFEH
DPRAM               EQU         0B800H
WD                  EQU         0B000H
ACKNOWLEDGE         EQU         0BFEAH
CONTROL             EQU         0BFECH
STATUS              EQU         0BFEEH
BEAMREFPORT         EQU         3038H
ZONEIA              EQU         3040H
ZONEEA              EQU         3048H
ZONEIB              EQU         3050H
ZONEEB              EQU         3058H
MCURESET1           EQU         201CH
MCURESET2           EQU         281CH
;
;
;
;
;
; PARAMETERS (RAM 100-200H)
; ==========
DATA        SEGMENT AT 0
            ORG     100H
FRAME       DW          ?           ;frame count
ROTATION            DB          ?           ;rotation count
                    DB          ?
SWEEP       DB          ?           ;sweep count
                    DB          ?
GUNSTAT             DB          ?           ;gun selected
                    DB          ?
```

```
FREQUENCY   DB          ?           ;frequency range 0,1,2
            DB          ?
SLOWFAST    DB          ?           ;0-slow,1-fast sweeps
            DB          ?
BEAMPOFF    DB          ?           ;beam processing off
            DB          ?
LFPOFF      DB          ?           ;lf    :    :
            DB          ?
HFPOFF      DB          ?           ;hf    :    :
            DB          ?
LFUNIT      DB          ?           ;lf unit to o/p
            DB          ?
HFBEN       DB          ?           ;hf energy group to op
            DB          ?
HFBNO       DB          ?           ;hf unit to o/p
            DB          ?
HFSTFM      DB          ?           ;hf e/unit
            DB          ?
LFSTFM      DB          ?           ;lf unit
            DB          ?
OUTMON      DB          ?           ;o/p frame monitor
            DB          ?
PROCMON     DB          ?           ;stats process monitor
            DB          ?
LASTE       DB          ?           ;previous e step
            DB          ?
NEWE        DB          ?           ;new e step
            DB          ?
LFOUTNO     DB          ?           ;lf frame o/p account
            DB          ?
HFOUTNO     DB          ?           ;hf  :   :   :
            DB          ?
BEAMOUTNO   DB          ?           ;beam :   :   :
        DB  ?
STATOUTNO   DB          ?           ;stats    :   :
            DB          ?
ZONE        DB          ?           ;zone selection
            DB          ?
UNIT        DB          ?           ;loop count
            DB          ?
UNIT1       DB          ?           ; :  :  :
            DB          ?
MAT         DB          ?           ;interrupt mask copy
            DB          ?
MODE1CNTR   DB          ?
            DB          ?
MODE2CNTR   DB          ?
            DB          ?
HFBCONCPY   DB          ?
            DB          ?
BEAMACTIVITY DB         ?
            DB          ?
MMUTESTNO   DB?         ?
            DB          ?
```

```
MMUTESTER   DB          ?
            DB          ?
FLYBACK     DB          ?
            DB          ?
LFAULT      DB          ?
            DB          ?
T1          DW          ?           ;beam stats params
T2          DW          ?
T12         DW          ?
C1          DW          ?
C2          DW          ?
C12         DW          ?
PEAK        DW          ?
LFBASE      DW          ?
;
        ORG 518EH ;STATS MONITORS
MON1        DB          ?
            DB          ?
MON2        DB          ?
;
;
DATA        ENDS
;
STACK SEGMENT AT 0
STACK ENDS
;
;   I/O ADDRESSES (accessed via ES)
;   ============
DATA1 SEGMENT       AT      1000H
        ORG     0 ;82C59 INT CONTROLLER
INT1_1      DB          ?
            DB          ?
INT1_2      DB          ?
;
        ORG 1800H   ;82C54-2 TIMER 2
            DB          ?
TIMER2_0    DB          ?
            DB          ?
TIMER2_1    DB          ?
            DB          ?
TIMER2_2    DB          ?
            DB          ?
TIMER2_CON  DB          ?
;
        ORG 4100H ;HF BOARD
HFBCON1     DB          ?
            DB          ?
HFBCON2     DB          ?
            DB          ?
HFBCON3     DB          ?
;
  ORG 2000H ;MCU BOARD 1
MCUCOM1     DB          ?
            DB          ?
```

```
MCUUCR1             DB          ?
                    DB          ?
MCUMCR1             DB          ?
                    DB          ?
MCUBRSR1            DB          ?
;
        ORG 2800H ;MCU BOARD 2
MCUCOM2             DB          ?
                    DB          ?
MCUUCR2             DB          ?
                    DB          ?
MCUMCR2             DB          ?
                    DB          ?
MCUBRSR2            DB          ?
;
        ORG 3000H ;BEAM BOARD
BEAMBASE            DB          ?
;
;
DATA1 ENDS
;
;
;     PSEUDO PROGRAM
;     ==============
;RESET (powerup,wd timer)     SERIAL INT
;INITIALISATION                serial data->ram
;stack setup                 RETURN
;cpu ram test
;interrupt vectors            ENERGY STEP INT
;segment pointers              update energy
;dpr test                    hfb off if flyback
;interrupt controller          copy energy to
;serial controller            hfb,mmuboards 1,2
;mmu reset/selfcheck            sum gun activity
;(timers)                    process beam cntrs
;default parameter values      RETURN
;start wd timer
;    !                    DPR INTERRUPT
;    V                     MSB=FE
;MAIN PROGRAM                    O/P next frame
;wait until stats frame o/p      RETURN
; beam data statistics          MSB=C0
; LF data statistics             acknowledge
; HF data statistics             reset sweep
;wait until next o/p block       check o/p frame account
;LOOP MAIN PROGRAM                if end block reset
;                              accounts,mmuboards
;                              update slow/fast
;                              check mode cycle
;                              cycle zones
;                              cycle frequency ranges
;                              update gun select
;                             RETURN
;
```

```
;
;MMU --> SPACE TIMING:
;8051-
;INT0<-15uS->O/P Start<-12uS->ok for int0
;serial transmission-
;          I<----20uS-------->I
;8086-                    I<5uS>Int0
;
;about 40uS per byte  1088bytes takes 43.5mS
;
;
CODE   SEGMENT
ASSUME          CS:CODE,DS:DATA,ES:DATA,SS:STACK
.    ;     SHUTTLE TETHER MISSION
     ;     ======================
     ;
           ;     M.P.GOUGH  28 Feb 1990
     ;
     ;
     ; LAST REVISED 19 JUNE 1990
           ;
           ;  SOURCE=MCU.ASM
           ;
           ;
     ; SPREE INSTRUMENT - MANIFESTED FOR
     ;      FLIGHT ON SHUTTLE 1991
     ; LOCATED IN SHUTTLE BAY DURING TETHERED
     ; SATELLITE DEPLOYMENT & DURING ELECTRON
     ; GUN EMISSIONS
     ; TWO COMBINED ELECTRON & ION SPECTROMETERS
     ; (2ELECTRON+2ION)X3 ZONE DIRECTIONS -> 12MCU
     ;
     ; FREQUENCY RANGES 10,5,1.3KHz COVER
     ; ION CHARACTERISTIC FREQUENCIES ,
     ; LOWER HYBRID FREQUENCY & ALSO
     ; ELECTRON RADAR MODE
     ;
     ; MCU.ASM 80C31 SOURCE CODE
     ; FOR L.F. ACF'S
     ; 12 MCU'S CONTROLLED BY 80C86 CPU
     ;
     ;
     ;80c31 with 16MHz XTAL--> .75uS T state
     ;MCU=80C31uP + 8K X 8 ROM + 2K X 8 RAM
     ;int e0- request data byte serial out
     ;serial out- data out
     ;serial in -
     ;   00XXXXXX  energy 00-1fh+20h flyback
     ;   01000yxx  y=slow,0 fast,1
     ;             xx=00-10khz;01-5khz;10-1.3khz
     ;   11111111  data all read out,
     ;             o/p pointer reset->processing
     ;timer 0   - particle event counting
     ;timer 1   - sampling timing
```

```
;reset - fill ram with ramps=ls address
;
;
;Program takes samples while processing
;                previous data take
;Total processing time = 4.4ms
;Detection efficiency-
;  At 10kHz 72 per cent
;  At 1.3kHz and 5kHz about 99 per cent
;
;10kHz data take 3.2mS
; 5kHz data take 6.4mS
;1.3kHz data take 25.6mS
;Energy step 31mS(slow) and 4mS(fast)
;Constant energy level check only for
;slow stepping at 5 and 10kHz ranges
;
;
;     External RAM Use
;     ----------------
;0000-03ffh 32 energies x 32 point acf array
;0400-043fh 32 x ( ls + ms ) 16bit acfoffset
;(0000-043fh) is transmitted 1 byte/request
;0520-055fh 64 data count samples
;0700-0707h key parameters
;
;     Internal RAM Use
;     ----------------
;00-07h r0-r7 general registers
;08-1fh stack
;20-5fh copy of data take
;20-3fh superimposed separations
;60-7fh this process generated acf
;
;      Port 1 as monitor
;      -----------------
;Reset->ff  After Ram test ->00
;Bit 5=1 during processing of last data
;Bit 6=1 during o/p.
;Bit 7=1 during each sample take
;Bits 0-7 =serial i/p value
;
;     EQUATES (Key parameters)
;     ========
FREQUENCY   EQU 0700H          ;SLOW/FAST, FREQUENCY
NENERGY          EQU 0701H          ;NEW ENERGY STEP
THISE            EQU 0702H          ;THIS ENERGY FOR DATA TAKE
ACTUALE          EQU 0703H          ;ACTUAL ENERGY FOR PROCESS
ENDE             EQU 0704H          ;ENERGY AT END OF DATA TAKE
SAMPLEN          EQU 0705H          ;SAMPLE NUMBER
F1KC             EQU 0706H          ;EXTRA DELAY FOR 1.3KHZ
PREVIOUSSAMP     EQU 0707H          ;SAVE FOR COUNT CALCULATION
OPL              EQU 0708H          ;O/P POINTER L.S.
OPH              EQU 0709H          ;O/P POINTER M.S.
```

```
ENDOUT          EQU 070AH       ;O/P END FLAG
   ;       (Others)
PCON            EQU 87H         ;POWER CONTROL REGISTER
           ; (undefined in asm51)
DAR0            EQU 00H         ;R0 AS A DIRECT ,INTERNAL DATA RAM
DAR4            EQU 04H         ;R4 AS A DIRECT, INTERNAL DATA RAM
   ;
   ;   INTERRUPT VECTORS
   ;   ==================
 ORG 0000H
   AJMP START                    ;RESET ON POWERUP
 ORG 0003H
   AJMP OUTPUT                   ;INTERRUPT E0 -> OUTPUT DATA ARRAY
 ORG 000BH
   AJMP START                    ;NOT USED.
 ORG 0013H
   AJMP START                    ;NOT USED
 ORG 001BH
   AJMP T1INT                    ;TIMER 1 --> SAMPLE TAKE
 ORG 0023H
```

The SPACE boards have been verified with Amptek personnel during joint tests. Some communication problems were encountered, especially in the SPACE CPU to Low Frequency MCUs when the SPACE CPU is being accessed by the main SPREE CPU. After adjustment of the software loop times, this difficulty was successfully overcome. At the present time the flight boards are in transit to the UK for function verification here. After these tests they will be returned as soon as possible to the United States. Upon receipt there, the development/engineering boards will be returned to the UK for further software optimization. The only remaining problem is in switching between fast and slow stepping modes, since it causes the SPACE CPU to hang up. This switching is done numerous times during flight and the SPACE watch-dog timer recovers the situation within one second. Nevertheless, the problem ought to be solved to provide a complete understanding of the system.

One change that has been made recently was to include a neural network type approach for the real-time data stream. This stream has always been intended as a means of indicating the nature of the results being recorded on-board on the EXABYTE recorder for real-time decision making and function verification. The best way to achieve an 'intelligent data analyst' is by a pattern recognition system using neural networks. The network data is prelearned by ground PC (taking about 3 hours!) but the SPACE algorithm using this data set takes only a few tens of mS to apply it to a data set. The SPACE ROM easily has sufficient room for the neural network look-up data table.

Flight Data Recorder (FDR)

The flight data recorders were completed this reporting period. They have been hermetically tested, thermal vacuum tested, functionally tested, and vibrated to space shuttle qualification levels. They have passed all tests to date.

A bridge controller was designed and installed in the FDR units. The bridge controller uses a microcontroller unit to control the Small Computer Serial Interface (SCSI) that the data recorder uses. The bridge controller monitors temperatures and operates heaters if the FDR temperature falls below +5° C. It contains a pressure transducer to monitor the housing pressure. It accepts data from the DPU and buffers it to the helical tape recorder. The various status and operational signals from the tape recorder are processed by the bridge controller. Beginning of tape, end of tape, record positioning, rewinding and tape loading are performed by the bridge controller so that these functions are transparent to the DPU. The tape remaining information is monitored and transferred to the DPU. Errors, re-write attempts, bad tape indications, and fault conditions are monitored and corrective action attempted. The software necessary to handle these tasks was designed, written and tested. The following preliminary operating manual discusses in detail the operation of the FDR system:

1. Introduction

The Flight Data Recorder (FDR) for SPREE is a stand alone unit designed for the Shuttle environment. The modular construction of the FDR allows the unit to employ the most up to date technology while maintaining a consistent interface. Designers can specify the interface for long term programs and still take advantage of emerging storage techniques. Capacities of 2000 megabytes can be obtained with minimal housekeeping.

2. Cartridge Tape Subsystem (CTS)

The actual storage device is presently an Exabyte EXB-8200. Communication with the drive is via a SCSI interface. A full 1900 megabytes can by stored on the streaming tape in as little as 2 hours. The CTS handles error correction on the tape and keeps the undetected error rate to less than one bit in 10^{12}.

3. Bridge Controller (BC)

The BC connects the storage device to the outside world. All house keeping unique to the drive is handled by the BC. The Bridge Controller provides a consistent interface to equipment using the FDR.

3.1 Interface

The FDR communicates with a partial implementation of the MIL-STD-1553 bus. Data is Manchester encoded Bi-phase level type. Signals are transmitted on a differential wire pair. The coding scheme can differentiate between commands and data. A minimum implementation involves a 'Request To Transfer' and 'Clear To

Transfer' command/status handshake followed by a 'Transfer' command and a data block burst of predefined length. The SPREE DPU bursts sixteen 1024 byte blocks periodically every second.
SPREE carries two FDRs and occasionally broadcasts to both simultaneously. For this situation, the DPU arms both FDRs by implementing a unique handshake for each FDR. The DPU then sends a common trigger command followed by data. Status and house keeping data can also be requested by the DPU.

4. Operation

4.1 BC / CTS Interface

The BC connects to a SCSI bus as an initiator. The CTS responds as a target. Thus the CTS controls information exchange on the SCSI bus.
SCSI protocol requires the BC's SCSI Controller chip to arbitrate for the bus by asserting an I.D. of 7 (/DB7 line) and asserting the busy line. After gaining temporary control of the bus by default, the Controller asserts the target's I.D. of 0 (/DB0 line), negates the busy (/BSY) line and asserts the select (/SEL) line. When the CTS is ready, it will assert the busy line and take control of the bus. The CTS now dictates the command, status, data, and message transfer phases. Phases are interpreted by decoding the /CD, /IO, and /MSG lines.

4.1.1 Command Phase

After the BC selects the CTS, the CTS should request a command phase. All valid commands for the CTS consist of six bytes each. Hand shaking on the SCSI bus is by the /REQ line asserted by the CTS and the /ACK line asserted by the BC. Six /REQ & /ACK hand shakes are required to transmit each byte of the command. The command phase is always sends six bytes from the BC to the CTS.

4.1.2 Data Phase

If the command requires data transfer, the CTS will request a data phase. The data phase is Bi-directional and of variable length.

4.1.3 Status Phase

The status phase normally follows the command and optional data phase. This phase is equivalent to the command phase, but in the opposite direction. Typically, the CTS returns a 'good' status or a 'check condition' status. The status phase will always send one byte from the CTS to the BC.

4.1.4 Message Phase

The only message supported by the BC is 'command complete' from the CTS. For this reason, the BC must never assert the /ATN line. The 'command complete' message phase will always terminate a command sequence and imply a pending disconnection. The message phase will always send one byte from the CTS to the BC.

4.1.5 SCSI Commands

SCSI supported by the BC are as follows:

Test Unit Ready	(00h)
Rewind	(01h)
Request Sense	(03h)
Read	(08h)
Write	(0Ah)
Write Filemark	(10h)
Space	(11h)
Inquiry	(12h)
Mode Select	(1Ah)

4.1.6 SCSI Status

Status bytes recognized by the BC are as follows:

Good	(00h)
Check Condition	(01h)
Busy	(04h)

4.1.7 SCSI Messages

Messages recognized by the BC are as follows:

4.1.8 Sense Keys

Sense keys recognized by the BC are defined in Serial Subaddress 'Sense'.

4.1.9 SCSI Command Flowchart

The EXB-8200 requires specific handshaking and protocol. A state diagram for command and data transfer with the CTS follows. (Insert flowchart here)

4.2 Serial / BC Interface

4.2.1 Serial Protocol

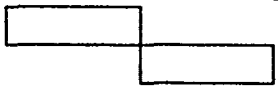
Control of the FDR is via the serial channel. Both the FDR and SPREE DPU will adhere to the following protocol. In MIL–STD–1553 terminology, each FDR is a remote terminal (RT) and the DPU is the bus controller (not a BC). The DPU sends command words and the FDR returns status words. Both are capable of transferring data when preceded by a command or status word.

4.2.1.1 Word Formats

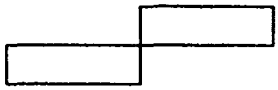
BIT TIMES

1	2	3

COMMAND/STATUS SYNC



DATA SYNC



BIT TIMES

4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

COMMAND WORD

5	1	5	5	1
REMOTE TERMINAL ADDRESS	T/R	SUBADDRESS	DATA WORD COUNT	P

DATA WORD

16	1
DATA	P

STATUS WORD

5	1	1	1	3	1	1	1	1	1	1
REMOTE TERMINAL ADDRESS	A	B	C	RESERVED	D	E	F	G	H	F

Remote Terminal Address:	The RT address for SPREE FDR A is 00000b. The RT address for SPREE FDR B is 00001b. Broadcast mode is enabled with an address of 11111b.
T/R:	Receive (DPU to FDR) is requested with a binary 0. Transmit (FDR to DPU) is signaled with a binary 1. This bit is used in conjunction with data transfer commands to indicate direction.
Subaddress:	Functions are specified in these five bits.
Data Word Count:	Data word count is entered in these five bits. A count of 11111b is 31. A count of 00000b is 32.
P:	Odd parity is used. If the number of bits in the 16 bit field is even, then the parity bit is set to 1.
Data:	The data transfer field.

A: The message-error bit is set to 1 after receiving an unrecognized command.

B: The instrumentation bit is always set to 1 after a write fault.

C: The service-request bit is set to 1 if the FDR requires attention. It is set after a power fault and is cleared by a rewind or append command. Recording is inhibited until the bit is cleared.

D: The broadcast-command-received bit is set after a broadcast data transfer and is readable with the next command/status phase.

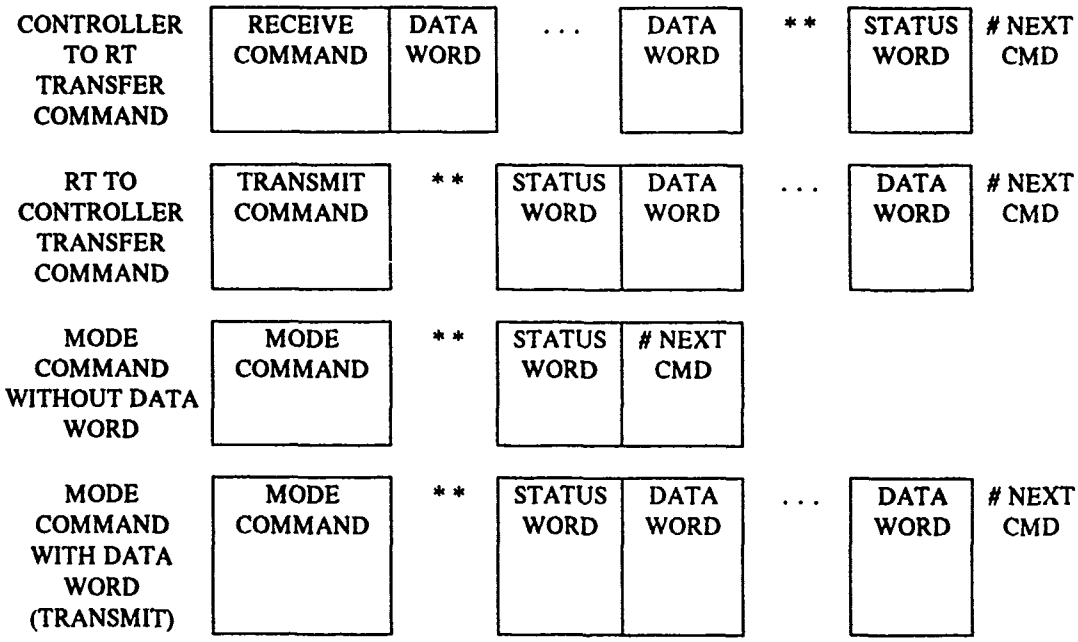
E: The busy bit is set to 0 to indicate that the FDR is ready to receive data. A 1 value indicates the FDR will ignore data.

F: The subsystem-flag set to 1 indicates that the BC detected a CTS fault. It is cleared by a successful read or write.

G: The dynamic-bus-control-acceptance bit is always set to 0.

H: The terminal-flag indicates a BC fault. A write timeout from the DPU is the only example.

4.2.1.2 Information Transfer Formats



NOTES: # INTERMESSAGE GAP
** RESPONSE TIME
For CONTROLLER read 'DPU'
For RT read 'BC'

Response times vary for different formats. Response to a receive subaddress must be short, on the order of a few milliseconds. Other subaddresses may allow delays of a second or two.

4.2.2 Serial Subaddresses

4.2.2.1 Request-To-Transfer (01h)

The request-to-transfer command is sent immediately before a transfer command. MIL–STD–1553 allows a maximum of 32 words to be sent with a transfer command. Amptek is extending this limit by specifying an additional five bits for the data word count. These extended bits are the MSB of the total data words transferred. This command also serves to notify the BC that a high speed data burst is pending. Current implementation of the BC only supports a value of 10000b (1024 bytes) for the data word count with this command.

4.2.2.2 Transfer (02h)

The transfer command precedes a data transfer. When used in conjunction with the request-to-transfer command, up to 2048 bytes may be transferred. Broadcast mode is supported by asserting all five bits of the terminal address. The data word count

provides the LSB of the total data words transferred. Current implementation of the BC only supports a value of 00000b for the data word count with this command and is interpreted as zero. A transfer command must be previously enabled by a request-to-transfer command.

4.2.2.3 Rewind (03h)

This command rewinds an FDR to its Logical Beginning of Tape (LBOT).

4.2.2.4 Append (04h)

The append command fast forwards the tape to the end of valid data. This command can be used to continue writing after an automatic rewind caused by a power failure.

4.2.2.5 Sense (05h)

This command returns five (5) words relating the status of the CTS.

Byte 0	Sense key
Byte 1	R/W error count MSB
Byte 2	R/W error count
Byte 3	R/W error count LSB
Byte 4	Sense byte 19
Byte 5	Sense byte 20
Byte 6	Sense byte 21
Byte 7	Remaining tape MSB
Byte 8	Remaining tape
Byte 9	Remaining tape LSB

4.2.2.6 Housekeeping (06h)

This command returns two (2) words relating the status of the BC.

Byte 0	Condition bits	
	Bit 0-3	Reserved
	Bit 4	Drive ready (1=ready, 0=not ready)
	Bit 5	Environment OK (1=ready, 0=not ready)
	Bit 6	Heater power (1=on, 0=off)
	Bit 7	Drive power (1=on, 0=off)
Byte 1	Case Temperature (80h=25°C)	
Byte 2	Drive Temperature (80h=25°C)	
Byte 3	Pressure (80h=760 torr)	

4.2.3 Serial Status

Serial status supported by the BC:
Clear To Transfer

4.2.4 Serial Command Flowchart

TBD (Insert flowchart here.)

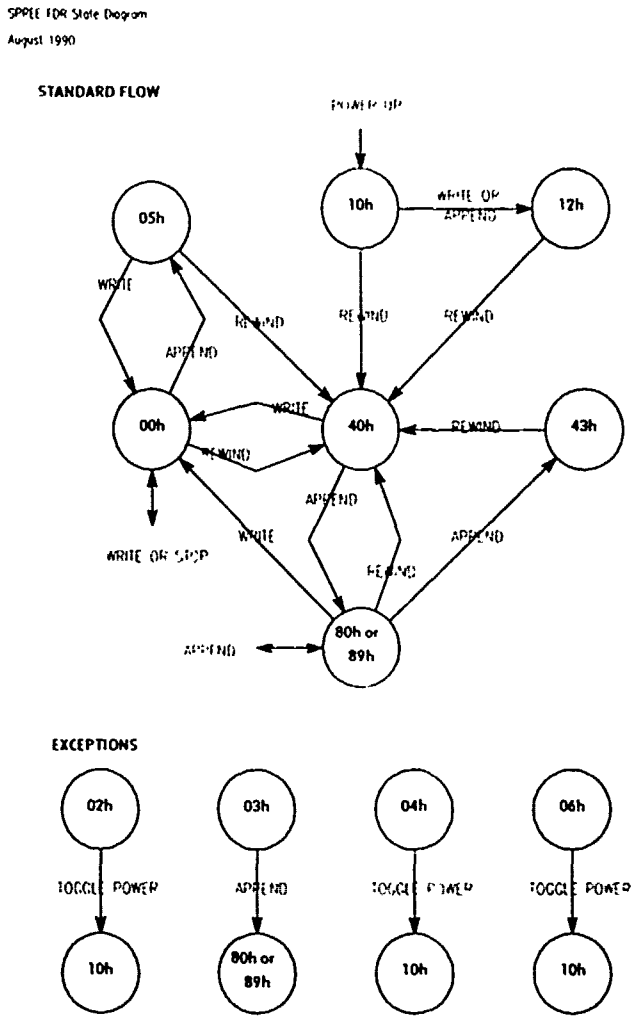
4.3 DMA Transfers

The BC is able to burst data between the serial port and RAM and between the SCSI controller and RAM. This is accomplished by DMA channel driven by the microcontroller. The DPU is able to quickly dump a block of data to the BC to be later loaded into the CTS.

DMA is not a typical feature of the 8051 microcontroller. The process is actually a high speed software loop that sequentially reads data into the microcontroller from a memory mapped device. A second memory mapped device is also enabled, but its write enable is ties to the microcontroller's read line. The microcontroller ignores the data read, but the cycle effectively transfers data from one memory mapped device to the next. The cycle can run within the 20μs required for each serial 16 bit word.

5. State Diagram

The BC polls each memory mapped device for activity, continuously servicing and updating status. A serial command with pending data holds the BC in a tight polling pattern on the serial port. This allows high speed data transfer.



Rotary Table Motor Drives

The Rotary Table Motor Drives (RTMD) were completed and tested during this year. Thermal modelling indicated that a high emissivity surface (black) would be preferable for temperature control. The RTMD is to be covered with a thermal blanket during flight and electrical surface conductivity is not an issue. We therefore decided to have a high emissivity flat black anodize surface applied to the RTMD. This worked well since it is a very hard surface and can be handled without damage. What wasn't anticipated was the high emissivity surface is somewhat rough as well as tough. This makes it difficult to clean since it abrades anything passed over its surface. Tissues and wipes shred as they wipe. Even skin contact leaves traces of debris which show up quite well against the black background. This isn't a serious problem; it just means that the RTMDs are difficult to clean and show dirt very easily.

Inside the RTMD housing is a flexible flat cable that connects to the ESA. This cable was made as a long flexible printed circuit board. Two problems occurred and were corrected with the assembly. A two sided flexible circuit is significantly more expensive than a single sided circuit. Therefore the circuit was designed as a single sided card. This results in mirror imaging the pin layout of the interconnected D connectors. This problem was corrected by wiring the short jumper that interconnects the ESA to the RTMD with another mirror image wired cable. This restores the correct pinout configuration.

The second ribbon problem that occurred was a manufacturing error that did not provide a stress relief pad on the solder lugs where they attached to the D connectors. This resulted in one line coming open after many hours of operation. The cables were returned to the manufacturer, who made new assemblies with appropriate stress relief. No further failures were experienced.

Another RTMD problem that occurred involved the grounding of the rotary table with its housing. Several measurements had been made of the harmonic drive impedance of $<0.1\ \Omega$ through its mounting. All those measurements were made while the table was not turning. We discovered the impedance varied from a few milliohms to hundreds of ohms while the table was moving! This problem was corrected by adding a heavy ground strap between the RTMD base plate and the moving table.

A motor control and display box was built and is being used for the RTMD testing. This box provides the proper step pulses and reversal commands that normally would be provided by the DPU. It also houses a pair of motor control boards to provide the raw stepping impulses to the stepping motors.

Vibration and thermal vacuum testing was conducted on the RTMDs without incident after properly setting the distance/sensitivity of the interrupter photodiode that is used to monitor table position and initiate reversal.

General SPREE Issues

A mock up of the SPREE Mounting Bracket was designed and built. This carrier proved very useful in the testing and development of the SPREE hardware. It

was used in some thermal vacuum testing. It was used to model and build the flight cables necessary for interconnecting the SPREE modules.

Building the flight harness proved to be a learning experience. Two problems surfaced; (1) some flight connectors were expensive, had minimum quantities of fifty, and very long lead times (>26 weeks), and (2) a shielded back shell assembly was necessary for the flight harness, but there was no commercial source of these backshells.

The first problem of the scarce expensive connectors was resolved by purchasing another manufacturers stainless steel shell mil spec connectors. These connectors are non-magnetic and composed of all flight approved materials, but are not listed on the Goddard QPL-19. There were no minimum quantities and the prices were much more realistic. Amptek decided to use the alternate connectors in order to meet delivery and cost constraints. Testing of these connectors has been successful.

The second problem of a shielded backshell was finally resolved by a visit to the Martin Marietta plant in Colorado. We were shown the tools and procedures they used to manufacture their own backshells. Armed with a copy of their procedure and notes from our visit we were able to build our own. Teflon mandrels had to be manufactured for each size connector shell had to be manufactured to allow solder tining of the shields and backshells. The backshells themselves posed cost and delivery constraints that jeopardized the schedule. We ended up purchasing mil-standard backshells made from cadmium plated steel. These shells were sent to a metal processor who stripped the cadmium plate away and re-plated them with gold. Since there is not a magnetic cleanliness requirement on SPREE, we decided to accept with the residual magnetism that the re-plated shell exhibited. The gold plating was sufficient to allow soldering to it and thereby allowing us to manufacture the required shielded backshells.

In early August we ran our first full-up operation of the entire SPREE experiment mounted on the SMB. The ESAs used the dummy MCP loads that had been prepared. After various small problems were identified and resolved, the instruments and software performed as desired.

After the full-up operation, the SPREE was taken for EMI/EMC testing. Generally speaking, the tests were successful but several emissions problems were identified. As the time for this report ends, Amptek is correcting some of the problems we observed. In particular we are adding ferrite beads to some of the low voltage power lines to suppress their radiation. We also are shielding the non-flight cables that are used to attach the SPREE to the GSE. These cables were not shielded since they are not flight hardware, but they must be shielded to survive EMI/EMC testing. A new series of EMI/EMC tests have been scheduled to test our re-work.